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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,150	09/17/2003	Mitsuyoshi Endo	04173.0437	4196

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,150	ENDO ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0903*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 09/17/2003 through 05/02/2005, claims 1-13 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 09/17/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-12, drawn to semiconductor devices, in the Response to Restriction Requirement filed 05/02/2005.

Claim 13 has been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim(s) 1 and 11 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by admitted prior art (Admission).

Regarding claim 1, Admission discloses a semiconductor device, as shown in figs. 21-22 of the pending application, comprising:

a wiring board 301;

a semiconductor chip 302 provided on said wiring board 301 and having a pad 303 electrically connected to a wiring on said wiring board 301; and

a second semiconductor chip 305 provided on said wiring board 301 at a position facing a side of said semiconductor chip 302, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring on said wiring board electrically connected to the pad of said semiconductor chip.

Regarding claim 11, Admission discloses a semiconductor package member, as shown in figs. 21-22 of the pending application, comprising:

a wiring board 301 on which a semiconductor chip 302 is mountable; and

an auxiliary semiconductor chip 305 provided on said wiring board 301 at a position facing a side of said semiconductor chip 302 to be mounted, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring on said wiring board.

7. Claim(s) 1-12 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,362,525 to Rahim.

Regarding claim 1, Rahim discloses a semiconductor device, as shown in figs. -10, comprising:

a wiring board 92 (fig. 9) or 104 (fig. 10);

a semiconductor chip 90 provided on said wiring board and having a pad electrically connected to a wiring on said wiring board 92/104; and

a second semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip 90, having passive elements integrated therein, and having pads 34 for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring 30, 32 on said wiring board 92/104 electrically connected to the pad 48 of said semiconductor chip 90.

See further col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 2, Rahim discloses the semiconductor device wherein the passive elements integrated in said second semiconductor chip are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Regarding claim 3, Rahim discloses a semiconductor device wherein said semiconductor chip 90 is flip-chip-connected to said wiring board 92/104 so as to electrically connect the pad to the wiring on said wiring board. See figs. 9-10. and col. 9, lines 41-65.

Regarding claim 4, Rahim discloses a semiconductor device wherein said semiconductor chip 90 has bonding wire connection to the wiring of said wiring board so as to electrically connect the pad to the wiring on said wiring board. See col. 9, lines 47-58.

Regarding claim 5, Rahim disclose a semiconductor device wherein said second semiconductor chip is flipchip-connected to said wiring board so as to electrically connect the pads for external connection to the wiring on said wiring board. See figs. 9-10.

Regarding claim 6, Rahim discloses a emiconductor device wherein said second semiconductor chip has bonding wire connection to the wiring of said wiring board so as to electrically connect the pads for external connection to the wiring on said wiring board. See col. 2, line 62 to col. 3, line 6; col. 9, lines 41-65; and col. 12, lines 14-34.

Regarding claim 7, Rahim discloses a semiconductor device wherein said semiconductor chip and said second semiconductor chip are both 60 μm or less in thickness. This is well known in the art. See also col. 2, lines 7-61.

Regarding claim 8, Rahim discloses a semiconductor device wherein said second semiconductor chip has, besides the pads for external connection used for the

flipchip connection to said wiring board, a pad for external connection not contributing to the flipchip connection to said wiring board. See col. 11, line 18 to col. 12, line 33.

Regarding claim 9, Rahim discloses a semiconductor device, as shown in figs. 3-10, comprising:

a plurality of semiconductor device portion units arranged in a lamination direction and each including:

a wiring board 92/104 (figs. 9-10);

a semiconductor chip 90 provided on said wiring board and having a pad electrically connected to a wiring on said wiring board 90; and

a second semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip 90, having passive elements integrated therein, and having pads 34 for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring 32 on said wiring board 92/104 electrically connected to the pad of said semiconductor chip 90; and

a vertical wiring portion 30 passing through said wiring boards 92/104 of said plural semiconductor device portion units and electrically connecting said wiring boards 92-104 to one another.

See further 7, line 55 to col. 8, line 22; col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 10, Rahim discloses a semiconductor device wherein the passive elements integrated in said second semiconductor chips of the respective plural semiconductor device portion units are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Regarding claim 11, Rahim discloses a semiconductor package member, as shown in figs. 3-10, comprising:

a wiring board 92/104 (figs. 9-10) on which a semiconductor chip 90 is mountable; and

an auxiliary semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip to be mounted, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring 32 on said wiring board 92/104.

See further 7, line 55 to col. 8, line 22; col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 12, Rahim discloses a semiconductor package member wherein the passive elements integrated in said auxiliary semiconductor chips are elements of ene kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
May 13, 2005